Notice of References Cited

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Reexamination
MATSUI ET AL.

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Page 1 of

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-2001/0020224	09-2001	Tomit	703/23
	В	US-2001/0049769	12-2001	Ono	711/118
	С	US-5,592,679	01-1997	Yung	712/23
	D	US-5,565,706	10-1996	Miura et al.	257/723
	E	US-6,634,017	10-2003	Matsui et al.	716/11
	F	US-6,864,710	03-2005	Lacey et al.	326/39
	G	US-6,574,590	06-2003	Kershaw et al.	703/28
	Н	US-6,247,084	06-2001	Apostol et al.	710/108
	1	US-5,896,521	04-1999	Shackleford et al.	703/21
	J	US-			
	К	US-			
	L	US-			
	М	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	Р	•				
	Q					
	R					
	S					
	Т					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Berekovic et al., "A core generator for fully synthesizable and highly parameterizable RISC-cores for system-on-chip designs", 8-10 Oct. 1998, Signal Processing Systems, 1998. SIPS 98. 1998 IEEE Workshop on , Pages: 561 - 568
	٧	Ghosh et al., "Hierarchical test generation and design for testability methods for ASPPs and ASIPs", 3, March 1999, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Volume: 18, Pages:357 - 370
	w	Gottlieb et al., "Clustered programmable-reconfigurable processors", 16-18 Dec. 2002, □□Field-Programmable Technology, 2002. (FPT). Proceedings. 2002 IEEE International Conference on , Pages:134-141
	х	Cook et al., "Mapping computation kernels to clustered programmable-reconfigurable processors", 15-17 Dec. 2003, Field-Programmable Technology (FPT), 2003. Proceedings. 2003 IEEE International Conference on , Pages:435-438

Notice of References Cited Application/Control No. | Applicant(s)/Patent Under | Reexamination | MATSUI ET AL. | Examiner | Art Unit | Page 2 of | P

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-			
	В	US-			*
	С	US-	-		
	D	US-			
	Е	US-			
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	G	US-			
	н	US-			
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	J	US-			
	К	US-			
	L	US-		,	
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	Р					
	Q				·	
	R					
	s					
	Т					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Morris et al., "A re-confiigurable processor for Petry net simulation", 4-7 Jan, 2000, System Sciences, Proceedings of the 33rd Annual Hawaii International Conference on, Pages:9 pp., vol.1
	V	Sanchez et al., "Static and dynamic confiigurable systems", June 1999, Compurters, IEEE Transactions on, Volume 48, Issue 6, Pages:556-564
	w	Morris et al., "A scalable re-configurable processor", Jan3 Feb. 2000, Computer Architecture Conferemce, 5th Australasian, Pages:64-73
	х	Petit et al.,"A new processor architecture exploiting ILP with a reduced instruction word", 12 Feb. 1998, High Performance Architectures for Real-Time Image Processing (Ref.No. 1998/197), IEEE Colloquium on, Pages: 2/1-2/5

Notice of References Cited

Application/Control No.

10/621,449

Examiner

Helen Rossoshek

Applicant(s)/Patent Under
Reexamination
MATSUI ET AL.

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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	Р					
	ø					
	R					
	S					
	Т					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Borgatti et al., "A reconfigurable system featuring dynamically extensible embedded microprocessor, FPGA and cestomizable I/O", 2002, IEEE Custom integrated circuits Conference, Pages 2-3-1 -2-3-4
	٧	Milligan et al., "Processor implementations using queues", Aug. 1995, Micro, IEEE, Volume 15, Issue 4, Pages: 58-66
	w	Benoit et al., "Metrics for reconfigurable architectures characterization: remanence and scalability", 22-26 April 2003, Parallel anddistributed processing symposium, Proceedings, International, Pages: 8 pp.
-	х	Memik et al., "An integrated approach for improving cache behavior", 2003, Design, Automation and test in Europe Conference and Exhibition, Pages 796-801

Notice of References Cited Application/Control No. 10/621,449 Examiner Helen Rossoshek Applicant(s)/Patent Under Reexamination MATSUI ET AL. Page 4 of 4

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-			
	В	US-			
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FOREIGN PATENT DOCUMENTS

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	R					
	Ø			·		
	Т					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Kastrup et al., "A novel approach to minimising the logic of combinatorial multiplexing circuits in product-term-based hardware", 2000, IEEE, Averito University, Portugal, Pages 164-171
	٧	Sasaki et al., "Reconfigurable synchronized dataflow processor", 2000, IEEE, Pages 27-28
	W	Barat et al., "Software pipelining for coarse-grained reconfigurable instruction set processors", 2002, Peoceedings of the 15-th International Conference on VLSI design, IEEE, Pages:
	x	